ABSTRACT OF THE DISCLOSURE

In a CDR (clock data recovery) deserializer, a clock divider receives a recovered clock signal (SCLK) and generates a divided clock signal (RPCLK). The frequency of the divided clock signal is lowered with each cycle of the divided clock signal being generated for each count of cycles of the recovered clock signal up to a predetermined ratio number. A serial-to-parallel shift register shifts in recovered serial data bits with each cycle of the recovered clock signal and outputs the predetermined ratio number of the shifted recovered serial data bits at a predetermined transition of every cycle of the divided clock signal. A SYNC (synchronization) detect logic asserts a VRS (diVider ReSet) signal coupled to the clock divider for controlling the clock divider to generate the predetermined transition for a cycle of the divided clock signal when the VRS signal is asserted. The SYNC detect logic includes a plurality of reloadable register portions for storing a plurality of synchronization bit patterns for a plurality of communications protocol. Each of a plurality of bit pattern comparators inputs an intermediate parallel data output (IPDO) from the shift register with each cycle of the recovered clock signal and compares for every cycle of the recovered clock signal the shifted recovered serial data bits to each of the synchronization bit patterns. A multiplexer selects one of the outputs of the bit pattern comparators as the VRS signal depending on the communications protocol of the recovered serial data bits.